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1. (currently amended) A multi-layer semiconductor chip package, comprising:

a ~~first~~ plurality of pairs of conductors for carrying a plurality of first signals in a layer of a carrier of the package; and, wherein each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly, wherein

~~a second pair of conductors for carrying a second signal adjacent to the first pair of conductors in the layer, wherein the first and second pairs of conductors are configured such that~~ cross-talk between ~~the first and second~~ the adjacent pairs of conductors is substantially minimized without increasing a size of the package.

5. (currently amended) The package of claim [4] 1, wherein the ~~first and second~~ adjacent pairs of conductors are positioned orthogonally to each other.

6. (currently amended) The package of claim [4] 1, wherein the second adjacent pairs of conductors is are positioned to be equidistant to each other conductor ~~in the first pair of conductors~~.

7. (original) The package of claim 1, wherein the layer is near an interface between the carrier and a chip.

15. (currently amended) A connector capable of being coupled to a semiconductor chip package, comprising:

a ~~first~~ plurality of pairs of conductors for carrying a plurality of ~~first~~ signals in a layer of a carrier of the package; ~~and, wherein~~ each pair of conductors in the layer is positioned so that adjacent pairs of conductors affect each other evenly, wherein

~~a second pair of conductors for carrying a second signal adjacent to the first pair of conductors, wherein the first and second pairs of conductors are configured such that~~ cross-talk between ~~the first and second~~ the adjacent pairs of conductors is substantially minimized without increasing a size of the package.

17. (currently amended) The connector of claim ~~16~~ 15, wherein the second adjacent pairs of conductors is are positioned to be equidistant to each other ~~conductor in the first pair of conductors~~.

18. (currently amended) A method for providing a semiconductor chip package, comprising the steps of:

(a) providing a ~~first~~ plurality of pairs of conductors for carrying a first plurality of signals in a layer of a carrier of the package; ~~and, wherein each pair of conductors in the layer is positioned so that~~ adjacent pairs of conductors affect each other evenly, wherein

~~(b) providing a second pair of conductors for carrying a second signal adjacent to the~~

~~first pair of conductors in the layer, wherein the first and second pairs of conductors are configured such that~~ cross-talk between ~~the first and second~~ the adjacent pairs of conductors is substantially minimized without increasing a size of the package.

22. (currently amended) The method of claim ~~21~~ 18, wherein the ~~second~~ adjacent pairs of conductors is are positioned to be equidistant to each other ~~conductor in the first pair of conductors~~.

23. (original) The method of claim 18, wherein the layer is near an interface between the carrier and a chip.